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(54) Title: ACTIVE PIXEL SENSOR WITH FULLY-DEPLETED BURIED PHOTORECEPTOR
(54) Titre: DETECTEUR DE PIXELS ACTIFS A PHOTORECEPTEUR ENTERRE A DEPLETION COMPLETE

(57) Abstract

A fully depleted photodiode (200) accumulates charge into both the photodiode (200) and a separate floating diffusion (205). The photodiode (200) is a buried photodiode having two PN junctions for photocarrier conversion. The floating diffusion (205) has less capacitance than the overall photodiode, thereby resulting in a knee-shaped transfer characteristic for charge accumulation that results in a larger dynamic range. The floating diffusion (205) is connected to an output transistor (210). A reset transistor has a gate (206) that is activated to connect the floating diffusion (205) to a diffusion region (208) that is held at VDD to reset the photodiode (200).

(57) Abrégé

Une photodiode (200) à déplétion complète accumule une charge à la fois dans ladite photodiode (200) et dans une région de diffusion flottante séparée (205). La photodiode (200) de type enterré possède deux jonctions PN qui permettent la conversion d'un photoporteur. La région de diffusion flottante (205) présente une capacitance inférieure à celle de la photodiode globale, ce qui produit une caractéristique de transfert en forme de genou permettant d'accumuler une charge qui produit une plage dynamique plus grande. La région de diffusion flottante (205) est connectée à un transistor de sortie (210). Un transistor de remise à l'état initial possède une grille (206) qui est activée afin de connecter la région de diffusion flottante (205) à une zone de diffusion (208) qui est maintenue au niveau de VDD, afin de remettre la photodiode (200) à l'état initial.

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(63) Related by Continuation (CON) or Continuation-in-Part (CIP) to Earlier Application
US Not furnished (CON)
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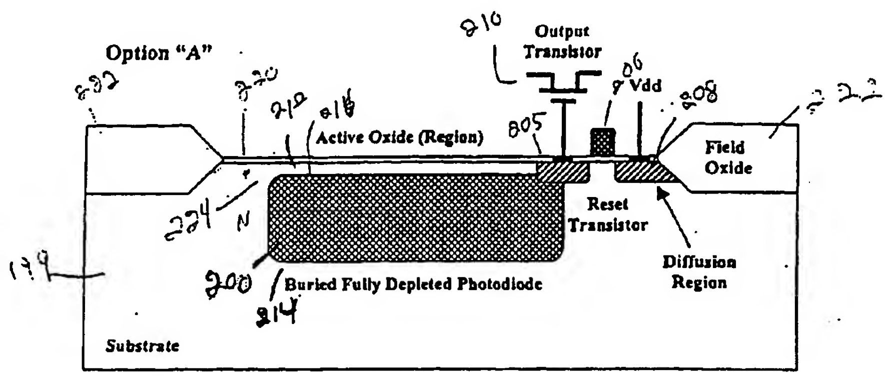
Published
With international search report.

(54) Title: ACTIVE PIXEL SENSOR WITH FULLY-DEPLETED BURIED PHOTORECEPTOR



(57) Abstract

A fully depleted photodiode (200) accumulates charge into both the photodiode (200) and a separate floating diffusion (205). The photodiode (200) is a buried photodiode having two PN junctions for photocarrier conversion. The floating diffusion (205) has less capacitance than the overall photodiode, thereby resulting in a knee-shaped transfer characteristic for charge accumulation that results in a larger dynamic range. The floating diffusion (205) is connected to an output transistor (210). A reset transistor has a gate (206) that is activated to connect the floating diffusion (205) to a diffusion region (208) that is held at VDD to reset the photodiode (200).

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Description

ACTIVE PIXEL SENSOR WITH FULLY-DEPLETED BURIED PHOTORECEPTOR

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims benefit of U.S. Provisional application No. 60/122,217, filed March 1, 1999.

BACKGROUND

Active pixel sensors are well known in the art. The basic active pixel sensor is described in U.S. Patent No. 5,471,515.

Active pixel sensors can use different kinds of active elements as their charge receiving elements. FIGS. 1A - 1C show three different examples of three of the common image sensing active elements.

A basic photodiode active pixel is shown in FIG. 1A. This includes a photodiode 100 on the substrate below an active oxide 102. The photodiode is connected directly to an output transistor 104. A gate 106 connects the photodiode 100 to a diffusion region 108 that is held at a voltage VDD.

The photodiode can be reset by activating gate 106, connecting the photodiode to VDD. Subsequent accumulation of charge changes the voltage on the photodiode.

The basic photogate active pixel sensor is shown in FIG. 1B. The active photogate 120 connects to the output transistor 122 through a transfer gate 124. This facilitates correlated double sampling in which the level of the photogate is first tested, then charge is transferred, and the value obtained again. Only the difference between the two charge amounts are used as an indication of the output. Hence, the output better indicates the amount of photogenerated electrons.

FIG. 1C shows the so-called pinned photodiode being used as an active element in an active pixel sensor. The pinned photodiode is shown in U.S. Patent No. 5,625,210. A transfer gate with channel implant 140 is used to transfer the charge out of the photodiode 142. The channel implant is used to adjust the bias of the pinned photodiode to facilitate charge output.

SUMMARY

The present system teaches using a fully-depleted buried photoreceptor with a coupled floating diffusion. The photoreceptor can be a "buried" diode, with an overlying portion of substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects will be described in detail with reference to the accompanying drawings, wherein:

FIGS. 1A - 1C show prior photosensitive elements as used in active pixel sensors;

FIG. 2A shows a photosensor of an embodiment in which the output transistor is directly connected to the photosensor;

FIGS. 2B - 2D show potential level diagrams for such a device;

FIG. 3 shows an alternative system in which a transfer gate is used to support correlated double sampling

FIG. 4 shows a fabrication layout of the system using a P-type buried photosensor with an N-well and a P-well; and

FIG. 5 shows a N-type buried device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment uses a fully depleted buried photodiode 200 as the photosensitive element. This photodiode is connected to a floating diffusion 205. That diffusion forms the output, either directly or via a transfer gate. The floating diffusion 205 is connected

to an output transistor 210, e.g. a transistor that is configured as a source follower. A reset transistor 205 has a gate 206 that is activated to connect floating diffusion to a diffusion region 208 that is held at VDD. This resets photodiode 200. The floating diffusion with reset transistor forms a vertical diffusion shield 600 located between the depleted photodiode 200 and the diffusion region 208. This is shown in Figure 2B.

The buried photodiode has two PN junctions for photocarrier conversion. Assuming that the buried photodiode 200 is of N-type, there is a first PN junction between the P-type substrate material 212 above the photodiode and the N-type photodiode itself. A second PN junction exists between the N-type photodiode 200 and the underlying P-type material 214. The two PN junctions have different photosensitivities in specific spectral ranges. For example, the upper PN junction near 212 may increase the photosensitivity to blue and green. The lower PN junction may increase the photosensitivity to green and red. These surface components can constitute one of the largest sources of leakage current for PN junction technologies. In addition, the dark current can be reduced by eliminating certain surface components.

The two different embodiments are optimized for different applications. The first embodiment is shown in Figure 2A. A silicon substrate 199 has a buried, fully depleted photodiode 200 formed therein. For purposes of this illustration, the photodiode will be assumed to be of N-type, in a P-type substrate. A layer of P material 212 overlies the top surface 216 of the photodiode, and the P-type material 199 surrounds all sides of the fully depleted photodiode.

The upper surface of the silicon includes an active oxide region 220, and a field oxide region 222. A space 224 is left between the edges of the photodiode 200 and the field oxide 222. This space 224 has been found to avoid mechanical stresses from the field oxide.

In the Figure 2 embodiment, the floating diffusion region 205 is connected directly to the photodiode 200. This floating diffusion region 205 can have the same impurity as the buried photodiode but at a higher concentration. The floating diffusion 205 is also connected to the output transistor 210. In addition, the floating diffusion is connected through a surface gate 206 to a diffusion region 208 that is biased at VDD.

Operation is shown in Figures 2B and 2C. Actuating the reset gate 206 brings the floating diffusion 205 to

VDD, thereby lowering the vertical diffusion shield 600, and allowing any charge in the photodiode (shown as 602) to dump into the diffusion region 604. Turning off the reset transistor 206 again raises the vertical diffusion bridge 600, and thereby again causes the charge to accumulate.

The charge accumulation occurs in two different stages which produces effectively a knee-shaped response slope. The slope of Voltage out as a function of incoming light is shown in Figure 2D. The first slope 610 occurs during the first part of the signal accumulation. During the part, the charge can accumulate in a relatively small "bucket", shown as portion 606. This small bucket represents the floating diffusion. This relatively small bucket has low capacitance, and hence can accumulate the charge particles quickly. This charge accumulates in the small bucket, according to a first response slope shown as the first slope portion 610.

Once the small bucket portion is filled (effectively the floating diffusion 205 is filled with charge), then charge begins accumulating in the higher-potential buried diode portion 200. This charge accumulation is held in a larger bucket. The accumulation in the larger bucket is

shown as 614. The operation produces a voltage-to-light transfer characteristics of a second slope 612.

The knee-shaped accumulation can be used for certain advantageous operations. A reason for obtaining the knee-shaped accumulation in this embodiment, however, is to compress the higher light portion, and accentuate the lower light portion. This enables the system to therefore obtain a larger dynamic range.

A second embodiment is shown in Figure 3. In this embodiment, a separate floating diffusion 305 is in contact with the buried fully depleted photodiode 200. A separate input transistor 308 separates between the floating diffusion 305 and the output floating diffusion 205 connected to output transistor 210. The output floating diffusion 205 is also connected to the diffusion region in a similar way to that described above in the Figure 2 embodiment. The input transistor 308 can be used to separate the two processes of photocharge integration and signal charge readout to facilitate correlated double sampling in order to reduce the KTC noise and parallel shutter. Like in the first embodiment, this system uses a controllable vertical diffusion bridge 305 to control the charge from the fully depleted photodiode. This system also leaves a space 224

between the top surface of the photodiode and the silicon substrate, thereby providing the same material as the silicon substrate above the photodiode as below the photodiode.

Implementation is shown in Figures 4 and 5, which show the wells that are used and the masks used to form those wells. Figure 4 shows a deep buried photodiode using an N-well. In this embodiment, the photodiode is buried more deeply. Figure 5 shows a shallow buried photodiode using a P-well. As discussed above, the shallow and deep burying at the wells can be used for different purposes.

Correlated double sampling occurs as follows. First, the whole system is reset by turning on the reset transistor gate 206 at the same time that the input transistor gate 310 is activated. This has the effect of resetting the floating diffusion 205, the second floating diffusion 305, and the buried fully depleted photodiode 200. After that, the gate 206 is turned off to raise the vertical diffusion bridge. At that time, the output transistor 210 is used to sample the value on floating diffusion 205. This represents the reset level. The output transistor 308 is then turned off, and charge is allowed to accumulate. At the end of the charge

accumulation, the output transistor 308 is turned back on, allowing the output transistor 210 to sample the value of charge stored in the photodiode.

This system enables increasing the quantum efficiency or spatial resolution. Since the spatial resolution is proportional to the pixel size, this system could obtain an increased internal gain.

Although only a few embodiments have been described in detail above, other embodiments are contemplated by the inventor and are intended to be encompasses within the following claims. In addition, other modifications are contemplated and are also intended to be covered.

Claims

What is claimed is:

1. A photosensor comprising:

a semiconductor substrate;

a buried photodiode in said semiconductor substrate, having a top surface which is separated from a surface of the substrate by a first area of the substrate, and a bottom surface which contacts said substrate; and

a photocarrier reading element which has a transfer curve with a first portion for a first part of the light, that has a first slope, and a second portion for a second part of the light that has a second slope, where said second slope is less gradual than said first slope.

2. A photo sensor as in claim 1 wherein said photocarrier reading element includes a floating diffusion, wherein said floating diffusion fills with charge to produce said first slope, and said photodiode fills with charge to produce said second slope.

3. A photosensor as in claim 2 further comprising a controllable vertical diffusion bridge to control accumulation exchange in said photodiode.

4. A photosensor as in claim 3 wherein said controllable vertical diffusion bridge is formed by a reset transistor.

5. A photosensor as in claim 2 further comprising a second diffusion region, separating said photodiode from said floating diffusion region.

6. A photosensor as in claim 5 further comprising a controlling transistor, controlling whether said first diffusion region will be coupled to said floating diffusion region.

7. A photosensor as in claim 3 wherein said substrate is a continuous material from said first area to said bottom area.

8. A photosensor as in claim 3 further comprising an output transistor, configured as a follower, and connected directly to said floating diffusion.

9. A photosensor comprising:

a semiconductor substrate having an upper surface;

a photodiode, which is fully depleted, is formed of a first conductivity type material, and is buried below said upper surface to leave a portion of the substrate over the photodiode and a portion of the substrate below the photodiode;

a floating diffusion region, formed of the same conductivity type of material as the photodiode, and coupled to the photodiode; and

a reset element, selectively erecting a vertical diffusion bridge, which when lowered, allows charge in the photodiode and floating diffusion to spill to and which when raised maintains charge in said floating diffusion and photodiode.

10. A photosensor as in claim 9, wherein said semiconductor substrate is an opposite conductivity type to said photodiode.

11. A photosensor as in claim 9, further comprising a second diffusion, coupled to said photodiode; and

a transistor separating between said second diffusion and said floating diffusion region, said second transistor selectively turned on to transfer charge to said floating diffusion region.

12. A photosensor as in claim 9 further comprising a reset diffusion and said reset element is lowered to transfer charge to said reset diffusion.

13. A method comprising:

using a buried photodiode to accumulate charge in a way that produces a transfer characteristic having a first steeper slope for lower light levels and a second more gradual slope for higher light levels.

Prior Art

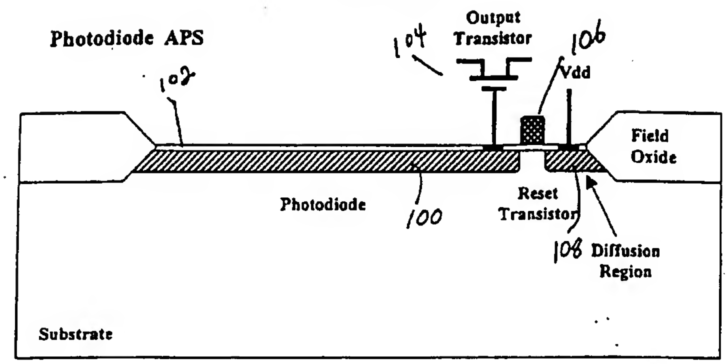


FIG 1A

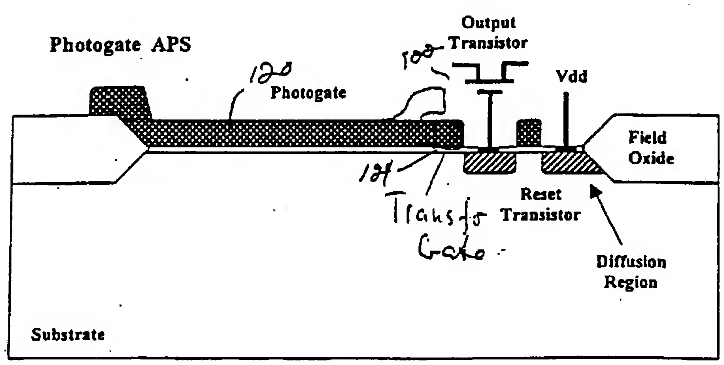


FIG 1B

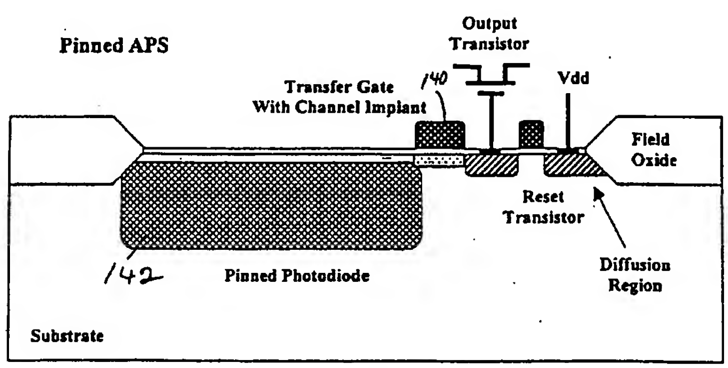
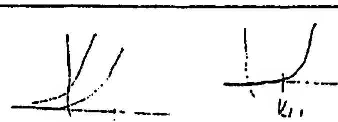


FIG 1C



Option "A"

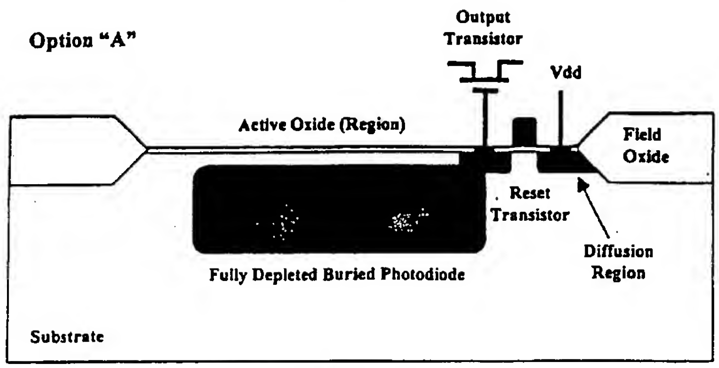


FIG 2A

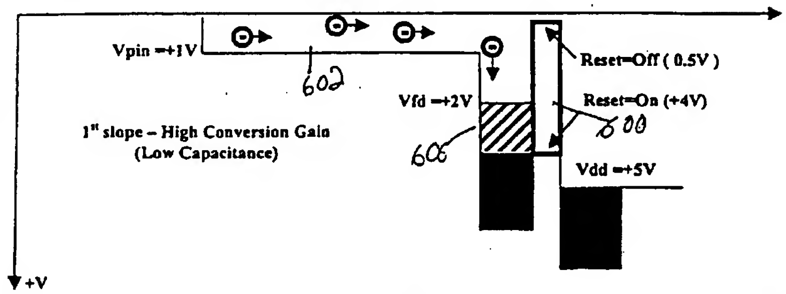


FIG 2B

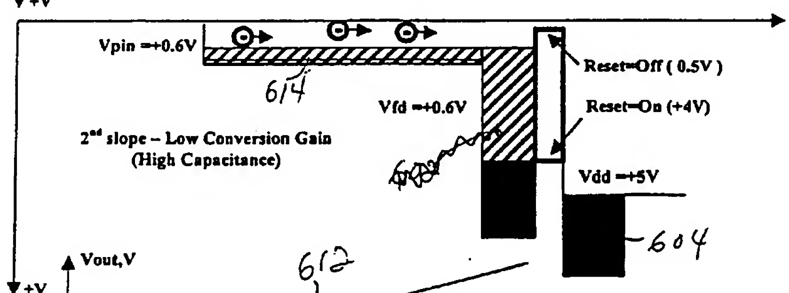


FIG 2C

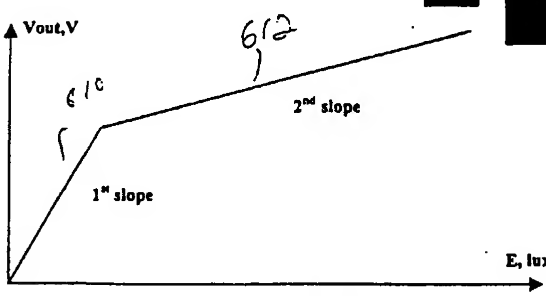


FIG 2D

Option #1 - Deep Buried Photodiode that used N-well;
Option #2 – Shallow Buried Photodiode that used P-well.
Both these options don't need special mask to reduce threshold voltage for recharged transistors.

As a result the quantum efficiency or space resolution may be increased. For image sensors the space resolution is inversely proportional to the pixel size. It is expected to obtain a smaller output capacitance and increased internal gain.

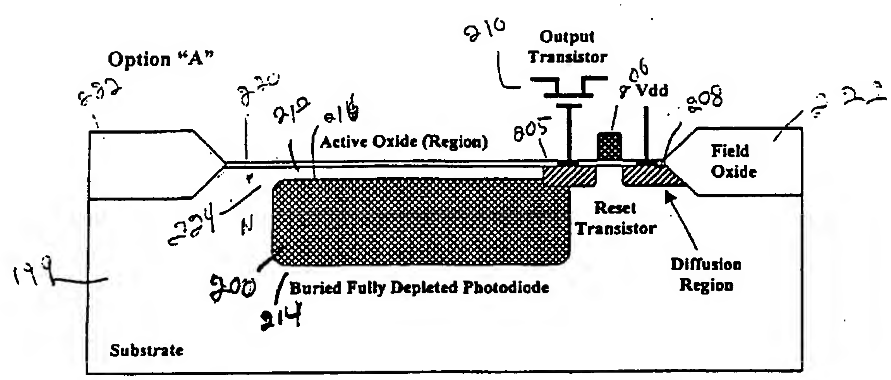


Fig 2A

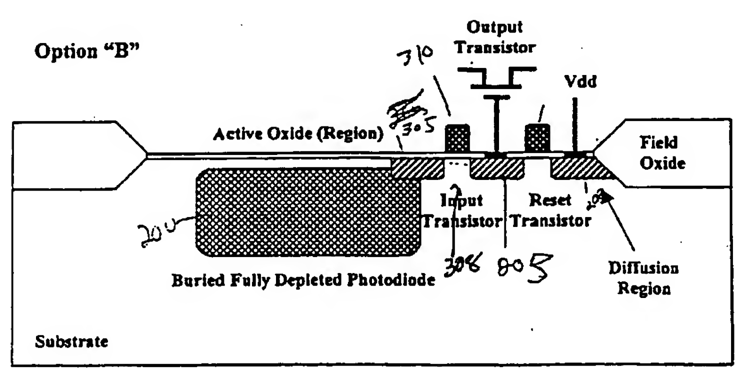


FIG 3

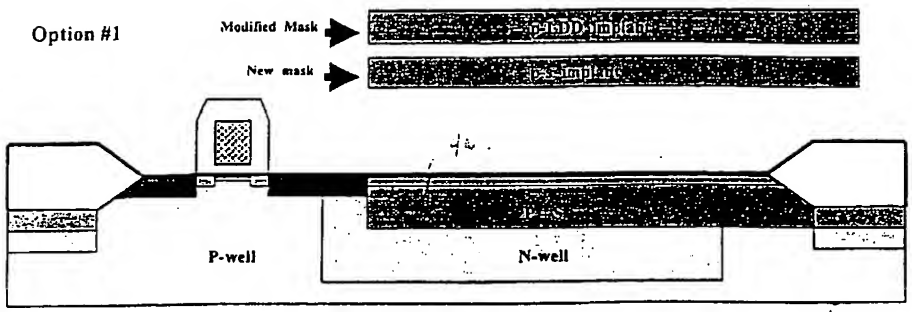

Option #1
Modified Mask
p-LDD implant
New mask
p-s implant
P-S
P-well
N-well

FIG 4

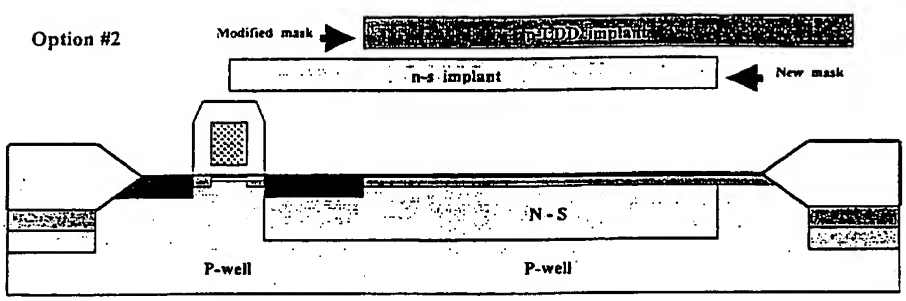

Option #2
Modified mask
p-LDD implant
n-s implant
New mask
N-S
P-well
P-well

FIG 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/05545

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) :H01L 31/06; 31/10
US CL :250/214.1; 257/292
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 250/214.1; 257/292; 250/208.1, 214R; 257/290, 291, 233, 234, 239

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X, P	US 5,903,021 A (LEE ET AL) 11 May 1999 (11/05/99), see entire document.	1-13
X	US 5,625,210 A (LEE ET AL) 29 April 1997 (29/04/97), see entire document.	1-13
A	US 5,471,515 A (FOSSUM ET AL) 28 November 1995 (28/11/95), see entire document.	1-13

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